



Title	ANALYSIS OF A CONTROLLER-BASED ALL-DIGITAL PHASE-LOCKED LOOP
Author(s)	Radhapuram, Saichandrateja; Bae, Jungnam; Jo, Ikkyun et al.
Citation	Far East Journal of Electronics and Communications. 2015, 15(1), p. 57-73
Version Type	VoR
URL	https://hdl.handle.net/11094/52099
rights	© 2015 Pushpa Publishing House
Note	

The University of Osaka Institutional Knowledge Archive : OUKA

<https://ir.library.osaka-u.ac.jp/>

The University of Osaka



ANALYSIS OF A CONTROLLER-BASED ALL-DIGITAL PHASE-LOCKED LOOP

**Saichandrateja Radhapuram, Jungnam Bae, Ikkyun Jo,
Weimin Wang and Toshimasa Matsuoka**

Graduate School of Engineering

Osaka University

2-1 Yamada-oka, Suita-shi

Osaka 565-0871, Japan

e-mail: teja@si.eei.eng.osaka-u.ac.jp

matsuoka@eei.eng.osaka-u.ac.jp

Abstract

A design procedure of an all-digital phase-locked loop (ADPLL) based on phase selection mechanism with loop stability independent of process, supply voltage and temperature is presented. A poly-phase filter and a phase interpolator are used to generate multiple phases to reduce the phase error. The modeling of proposed ADPLL structure is extensively investigated and mathematically described. For a phase and a frequency step input change, the closed-loop system of the proposed ADPLL eliminates phase error. Time-domain response of the behavioral-level simulation of the proposed structure on 130-nm CMOS technology with 0.7V supply voltage reveals the presented analytical model.

1. Introduction

The recent and ongoing explosive growth of wireless communication

Received: May 12, 2015; Accepted: June 2, 2015

Keywords and phrases: all-digital phase-locked loop, phase interpolator, z -domain, s -domain, steady-state error.

systems requires low-cost, low-voltage and low-power transceivers. The digital baseband applications are integrated in the most recent CMOS technology, while analog design is becoming increasingly difficult due to shrinking voltage headroom. Therefore, the implementation of wireless transceivers on a single chip requires digital realizations of analog functions [1, 2]. A digital intensive approach provides several additional advantages: improved reusability with optimized area and power dissipation, higher degree of integration, and the use of automated computer-aided design tools [3]. Shifting analog functions into the digital domain, however, is no straightforward task from viewpoints of design, simulation, and analysis techniques.

Phase-locked loops (PLLs) are essential parts of wireless communication systems, and are used to generate local-oscillator (LO) signal in modulation and demodulation. Although PLLs were originally purely analog devices, functional parts have been migrating step-by-step into digital domain. In recent days, all-digital phase-locked loops (ADPLLs) [3] have attracted a lot of attention. Conventional analog PLLs have a phase-frequency detector (PFD), charge pump, an analog loop filter, and a voltage-controlled oscillator (VCO). In typical ADPLLs, a time-to-digital converter (TDC), a digital loop filter, and digitally-controlled oscillator (DCO) replace the PFD, the analog loop filter, the VCO, respectively. From a circuit-level point of view, ADPLLs are digital systems because most of the components can be implemented with digital CMOS logic circuit. Some architectures aim to reduce the complexity of ADPLL structure by avoiding TDCs on account of increased noise level and spurs [4].

For several decades, the design and analysis of analog PLLs has been built up. Although ADPLLs have equivalent function of analog PLLs, design procedure and architecture are fundamentally different. To exploit the full possibilities of ADPLLs beyond the scope of traditional PLLs, an exact mathematical description is mandatory. While the number of ADPLL implementations is rapidly increasing [5-10], the number of analytical reports with system-level descriptions or design procedures is scarce. As traditional

PLLs, such as a charge-pump-based PLL, are inherently nonlinear systems [11], the phase-domain modeling is based on small-signal approximation that holds only in the close vicinity of the operational point, i.e., phase lock. On the other hand, ADPLLs aim to implement the linearized phase-domain model and are, therefore, ideally linear systems [12].

In this paper, we propose a TDC-less controller-based ADPLL structure. We utilize a poly-phase filter and a phase interpolator to generate multiple phases to reduce the phase error. A comprehensive mathematical modeling of proposed ADPLL with all discrete components running at fixed sampling rate is introduced. A major issue regarding the PLLs is the loop stability, which depends on the process, supply voltage and temperature (PVT). For the analog PLL, a self-biasing technology can be used to obtain PVT-independent stability [13]. For ADPLL, a gain normalization technology was proposed to make the loop-stability PVT-independent [12]. The proposed ADPLL structure with an additional phase selection loop makes the loop-stability PVT-independent.

This paper is organized as follows: the structure and operation of ADPLL are described in Section 2. Discrete-time z -domain and linear approximated s -domain models with loop stability and steady-state error analysis are presented in Section 3. Section 4 gives an insight into the time-domain behavior-level simulation of the ADPLL structure designed in 130-nm CMOS technology with a supply voltage of 0.7V and Section 5 draws the conclusions.

2. Controller-based ADPLL

The structure of the ADPLL proposed is shown in Figure 1(a). It has five major building blocks: PFD, controller, $\Delta\Sigma$ -modulator based DCO [3, 14], poly-phase filter (PPF) [15-17] and phase interpolator (PI) block [10, 18] followed by phase selector (PS), and frequency divider. The PFD detects both the phase and frequency difference between the two input signals. The pulses appearing at UP, DN relate to phase difference as in the conventional analog PLLs. The controller which can realize a function of a charge pump

and a loop filter as described later, accumulates the amount of these pulses at the DCO frequency, and generates two control words to tune the DCO frequency and the PS. Compared with the previous work using no TDC [9], this controller operates at the DCO frequency for precise phase difference detection. The phase selector selects one of multiple phases generated by the PPF and PI.

An n -stage PPF shown in Figure 1(b) is employed to get wide band to cover the tuning range of DCO [16]. To adjust the phase difference of the ADPLL directly and accurately, a resistor-based PI is adopted to reduce the power consumption as shown in Figure 1(c), which is similar to the interpolation technique used to reduce phase error in a folding interpolation analog-to-digital converter [19].

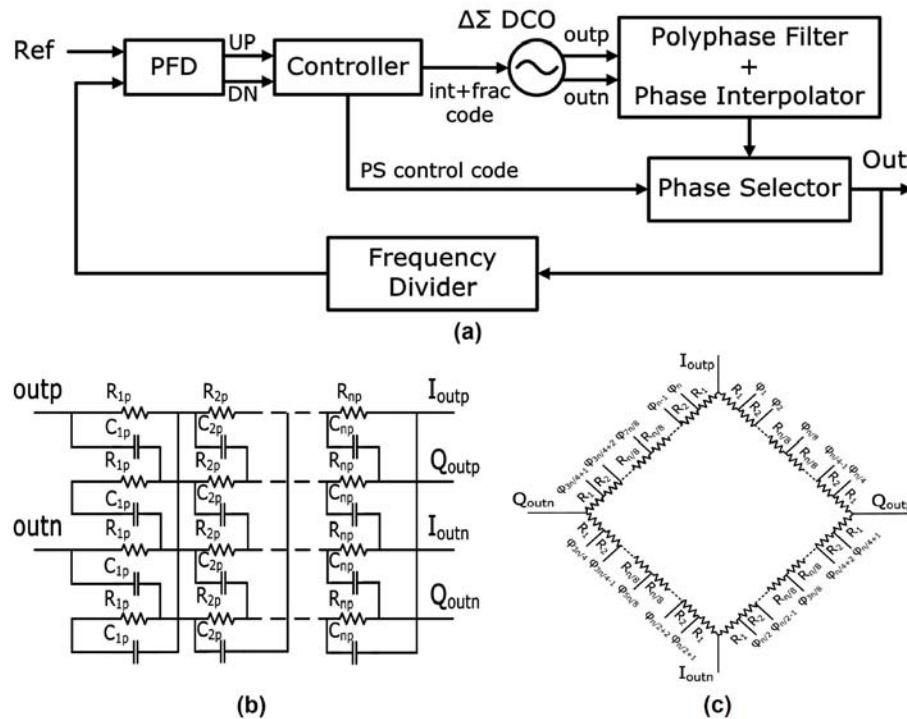


Figure 1. (a) Proposed controller-based ADPLL architecture, (b) PPF and (c) PI.

3. ADPLL Modeling in z - and s -domains

The z -domain representation and classical two-pole system theory can be used to analyze an ADPLL mathematically [12]. One similar mathematical analysis is performed here for the proposed ADPLL. All the discrete-time components in the proposed ADPLL operate at a fixed sampling rate of reference frequency. In order to simplify the model, an approximation of the uniform sampling or PLL update rate is used, despite the presence of small amount of jitter in the reference signal (Ref in Figure 1(a)).

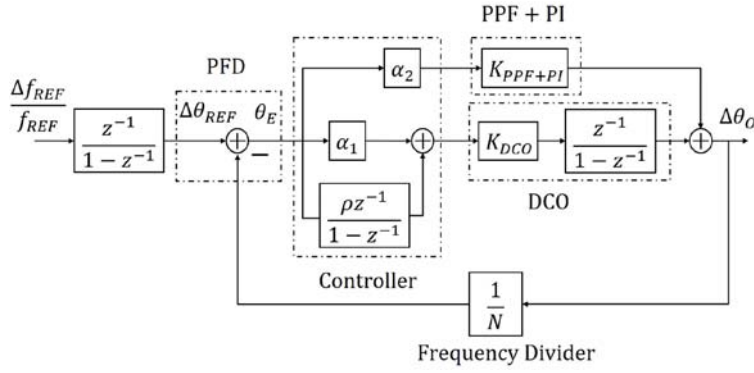


Figure 2. z -domain model of the proposed ADPLL architecture.

Figure 2 shows the z -domain model of the ADPLL architecture shown in Figure 1(a), where K_{DCO} represents the gain of DCO, K_{PPF+PI} corresponds to the factor from the $PPF + PI$ configuration, and N is the frequency division ratio. When the PPF and the PI generate M phases, $K_{PPF+PI} = 2\pi/M$. The $\Delta\theta_{REF}$ and $\Delta\theta_O$ are the excess reference and feedback phases for a change of Δf_{REF} of the reference frequency f_{REF} .

The controller has two transfer functions in discrete-time domain (z -domain) for the DCO and the phase selectors ($K_{CNT,DCO}(z)$ and $K_{CNT,PS}(z)$) as follows:

$$K_{CNT,DCO}(z)\theta_E(z) = 2^{-B_{frac}} \left[\frac{1}{M} \frac{z^{-1}}{1-z^{-1}} \left[\frac{N}{2\pi} \theta_E(z) \right] \right], \quad (1)$$

$$K_{CNT,PS}(z)\theta_E(z) = \frac{1}{M} \frac{z^{-1}}{1-z^{-1}} \left\lfloor \frac{N}{2\pi} \theta_E(z) \right\rfloor - \left\lfloor \frac{1}{M} \frac{z^{-1}}{1-z^{-1}} \left\lfloor \frac{N}{2\pi} \theta_E(z) \right\rfloor \right\rfloor, \quad (2)$$

where $\lfloor x \rfloor$ is the floor function, that is the largest integer not greater than x , B_{frac} is the digit number of fractional part of the DCO input, and $z = \exp(s/f_{REF})$. Within a small-signal analysis, to simplify the ADPLL analysis, the following approximations are used in this work:

$$K_{CNT,DCO}(z) \approx \alpha_1 + \frac{\rho z^{-1}}{1-z^{-1}} = \alpha_1 \frac{1 - (1 - \rho/\alpha_1)z^{-1}}{1-z^{-1}}, \quad (3)$$

$$K_{CNT,PS}(z) \approx \alpha_2. \quad (4)$$

The multiplication factors α_1 and ρ realize the same function as a charge pump and a loop filter, that is, generation of control signal of the DCO with a frequency response. For simplification of mathematical expressions, K_{DCO} and $1/N$ are scaled into the factors α_1 and ρ , and K_{PPF+PI} and $1/N$ are scaled into the factor α_2 , resulting in $\alpha_{1n} = K_{DCO}\alpha_1/N$, $\rho_n = K_{DCO}\rho/N$ and $\alpha_{2n} = K_{PPF+PI}\alpha_2/N$.

According to the signal and system theory, the open-loop transfer function $H_{ol}(z)$ can be expressed as

$$\begin{aligned} H_{ol}(z) &= \frac{\Delta\theta_O(z)/N}{\theta_E(z)} = \alpha_{2n} + \frac{\alpha_{1n}(z-1) + \rho_n}{(z-1)^2} \\ &= \alpha_{2n} \frac{z^2 + z\left(\frac{\alpha_{1n}}{\alpha_{2n}} - 2\right) + 1 + \frac{\rho_n - \alpha_{1n}}{\alpha_{2n}}}{(z-1)^2}. \end{aligned} \quad (5)$$

The closed-loop transfer function $H_{cl}(z)$ is obtained as

$$H_{cl}(z) = \frac{\Delta\theta_O(z)}{\Delta\theta_{REF}(z)} = \frac{NH_{ol}(z)}{1 + H_{ol}(z)}$$

$$= \frac{N\alpha_{2n}}{1 + \alpha_{2n}} \frac{z^2 + z\left(\frac{\alpha_{1n}}{\alpha_{2n}} - 2\right) + 1 + \frac{\rho_n - \alpha_{1n}}{\alpha_{2n}}}{z^2 + z\left(\frac{\alpha_{1n}}{1 + \alpha_{2n}} - 2\right) + 1 + \frac{\rho_n - \alpha_{1n}}{1 + \alpha_{2n}}}. \quad (6)$$

Although the z -transform is the natural description of a discrete-time system, it is common to approximate it with a linear continuous-time system in the s -domain. The accuracy of the linearization depends on the PLL bandwidth. The rule of thumb used in practice states that the input reference frequency f_{REF} must be at least 10 times larger than the PLL bandwidth [11], so that the approximation holds as

$$z = \exp(s/f_{REF}) \approx 1 + \frac{s}{f_{REF}}. \quad (7)$$

From equations (5) and (6), the open-loop and the closed-loop transfer functions in s -domain are obtained as follows:

$$H_{ol}(s) = \frac{\Delta\theta_O(s)/N}{\theta_E(s)} = \frac{\alpha_{2n}s^2 + \alpha_{1n}f_{REF}s + \rho_nf_{REF}^2}{s^2}, \quad (8)$$

$$H_{cl}(s) = \frac{\Delta\theta_O(s)}{\Delta\theta_{REF}(s)} = N \frac{\alpha_{2n}s^2 + \alpha_{1n}f_{REF}s + \rho_nf_{REF}^2}{(1 + \alpha_{2n})s^2 + \alpha_{1n}f_{REF}s + \rho_nf_{REF}^2}. \quad (9)$$

With the aid of linearized s -domain modeling, important control system characteristics are derived. For this phase model to be compared with the classical two-pole system transfer function, the phase error transfer function is expressed as

$$H_e(s) = \frac{\theta_E(s)}{\Delta\theta_{REF}(s)} = 1 - \frac{1}{N} H_{cl}(s) = \frac{1}{1 + \alpha_{2n}} \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}, \quad (10)$$

where the natural angular frequency ω_n and the damping factor ζ are given by

$$\omega_n = \sqrt{\frac{\rho_n}{1 + \alpha_{2n}}} f_{REF}, \quad (11)$$

$$\zeta = \frac{\alpha_{1n} f_{REF}}{2(1 + \alpha_{2n})\omega_n} = \frac{\alpha_{1n}}{\sqrt{4\rho_n(1 + \alpha_{2n})}}. \quad (12)$$

From equation (12), ζ only depends on α_{1n} , α_{2n} and ρ_n , implying that the loop stability of the ADPLL is independent of the input reference frequency, output frequency and PVT. Furthermore, according to the classical two-pole theory, the ratio of the loop bandwidth to natural angular frequency ω_n only depends on ζ . Equation (11) shows that the ratio of ω_n to the input reference frequency f_{REF} only depends on α_{2n} and ρ_n . Thus, the loop bandwidth tracks the reference frequency f_{REF} . This bandwidth-tracking feature can in turn provide broad operation frequency range. Thus, the ADPLL with phase selection mechanism has the same dependencies of ζ and ω_n on α_{1n} , α_{2n} and ρ_n , similar to the earlier ADPLLs reported in literature [12, 20].

3.1. Stability conditions of the ADPLL system

One mandatory requirement of designing ADPLL is that the system must be stable. Basically, the stable condition of a discrete-time system occurs when the roots of the characteristic equation are inside the unit circle $|z| = 1$ in the z -plane. One of the most efficient methods for testing the stability of a discrete-time system is Jury's stability criterion [21]. It can be applied directly to a second-order ADPLL model to determine the stable condition. According to the criterion, the necessary and sufficient conditions are that the characteristic equation of a second-order system

$$\Delta(z) = a_2 z^2 + a_1 z + a_0 = 0, \quad (13)$$

should meet the following conditions in order to have no roots on or outside the unit circle: $\Delta(1) > 0$, $\Delta(-1) > 0$ and $|a_0| < a_2$. Applying these conditions to the denominator of equation (6), where $a_2 = 1 + \alpha_{2n}$, $a_1 = \alpha_{1n} - 2(1 + \alpha_{2n})$ and $a_0 = 1 + \alpha_{2n} + \rho_n - \alpha_{1n}$, the necessary and sufficient stable condition ranges of this ADPLL architecture can be derived as $\rho_n > 0$, $\rho_n < \alpha_{1n}$, $\alpha_{1n} < \rho_n/2 + 2(1 + \alpha_{2n})$.

3.2. Steady-state error analysis of the ADPLL

The steady-state error analysis in terms of phase and frequency of the proposed ADPLL is carried out. It will be proven that both the phase and frequency errors of this ADPLL system will be zero when the system reaches steady state.

3.2.1. Phase step response

A step phase change of the input signal is expressed as $\Delta\theta_{REF}(t) = \Delta\theta u(t)$ in the time domain, where $u(t)$ is a unit step function and $\Delta\theta$ is the constant showing the phase step. Applying z -transform and Laplace transform to $\Delta\theta_{REF}(t)$ yields

$$\Delta\theta_{REF}(z) = \frac{\Delta\theta z}{z-1}, \quad (14)$$

$$\Delta\theta_{REF}(s) = \frac{\Delta\theta}{s}. \quad (15)$$

The phase error transfer functions in z - and s -domains, $\theta_E(z)$ and $\theta_E(s)$ can be written as

$$\theta_E(z) = \Delta\theta_{REF}(z) - \frac{\Delta\theta_O(z)}{N} = \left(1 - \frac{1}{N} H_{cl}(z)\right) \Delta\theta_{REF}(z), \quad (16)$$

$$\begin{aligned} \theta_E(s) &= \Delta\theta_{REF}(s) - \frac{\Delta\theta_O(s)}{N} \\ &= \left(1 - \frac{1}{N} H_{cl}(s)\right) \Delta\theta_{REF}(s) = H_e(s) \Delta\theta_{REF}(s). \end{aligned} \quad (17)$$

To confirm the steady-state error $\theta_E(t = \infty)$, the following final-value theorems in z - and s -domains are used:

$$\lim_{k \rightarrow \infty} \theta_E(kT) = \lim_{z \rightarrow 1} (1 - z^{-1}) \theta_E(z), \quad (18)$$

$$\lim_{t \rightarrow \infty} \theta_E(t) = \lim_{s \rightarrow 0} s \theta_E(s), \quad (19)$$

where $T = 1/f_{REF}$. The condition to use the former final-value theorem is that the function $(1 - z^{-1})\theta_E(z)$ has no poles on or outside the unit circle $|z| = 1$ in the z -plane. The conditions for the latter final-value theorem are that all poles of $\theta_E(s)$ have non-negative real parts and at most only one pole at origin.

Substituting equations (6), (14) and (16) into equation (18),

$$\begin{aligned} & \lim_{k \rightarrow \infty} \theta_E(kT) \\ &= \lim_{z \rightarrow 1} (1 - z^{-1}) \left(1 - \frac{1}{N} H_{cl}(z) \right) \Delta\theta_{REF}(z) \\ &= \lim_{z \rightarrow 1} (1 - z^{-1}) \frac{(z-1)^2}{(1 + \alpha_{2n})(z-1)^2 + \alpha_{1n}(z-1) + \rho_n} \frac{\Delta\theta_z}{z-1} = 0, \end{aligned} \quad (20)$$

and equations (10), (15) and (17) into equation (19),

$$\begin{aligned} \lim_{t \rightarrow \infty} \theta_E(t) &= \lim_{s \rightarrow 0} s H_e(s) \Delta\theta_{REF}(s) \\ &= \lim_{s \rightarrow 0} s \frac{1}{1 + \alpha_{2n}} \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \frac{\Delta\theta}{s} = 0. \end{aligned} \quad (21)$$

Based on the above analysis, the closed-loop system of the ADPLL eventually can eliminate the phase error for a step phase change in the input signal.

3.2.2. Frequency step response

A step frequency change of the input signal is expressed as $\Delta\theta_{REF}(t) = \Delta\omega t u(t)$ in the time domain, where $\Delta\omega$ is the constant showing the angular frequency step. The z -transform and Laplace transform of $\Delta\theta_{REF}(t)$ are given by

$$\Delta\theta_{REF}(z) = \frac{\Delta\omega T z}{(z-1)^2}, \quad (22)$$

$$\Delta\theta_{REF}(s) = \frac{\Delta\omega}{s^2}. \quad (23)$$

By using the final-value theorems (equations (18) and (19)), the steady-state error in time domain is obtained as follows:

$$\begin{aligned} \lim_{k \rightarrow \infty} \theta_E(kT) &= \lim_{z \rightarrow 1} (1 - z^{-1}) \left(1 - \frac{1}{N} H_{cl}(z) \right) \Delta\theta_{REF}(z) \\ &= \lim_{z \rightarrow 1} (1 - z^{-1}) \frac{(z-1)^2}{(1 + \alpha_{2n})(z-1)^2 + \alpha_{1n}(z-1) + \rho_n} \frac{\Delta\omega Tz}{(z-1)^2} = 0, \end{aligned} \quad (24)$$

$$\begin{aligned} \lim_{t \rightarrow \infty} \theta_E(t) &= \lim_{s \rightarrow 0} s H_e(s) \Delta\theta_{REF}(s) \\ &= \lim_{s \rightarrow 0} s \frac{1}{1 + \alpha_{2n}} \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \frac{\Delta\omega}{s^2} = 0. \end{aligned} \quad (25)$$

Hence, when the frequency of an input has a step jump, the ADPLL can eliminate any steady-state phase error and relock.

3.3. Comparison of transient and frequency responses

Figures 3(a) and 3(b) show the step response and magnitude response of closed-loop transfer functions $H_{cln}(z) = H_{cl}(z)/N$ and $H_{cln}(s) = H_{cl}(s)/N$. The magnitude response of the error transfer functions $H_e(z) = 1 - H_{cl}(z)/N$ and $H_e(s) = 1 - H_{cl}(s)/N$ is shown in Figure 3(c). The error transfer function gain factor $1/(1 + \alpha_{2n})$ corresponds to residual phase error. The residual phase error is nearly independent of the loop bandwidth within the parameter settings used in this work. Increasing the loop bandwidth of the PLL reduces the settling time. With the increase of the α_{2n} factor, there is a reduction in the residual phase error as shown in Figure 3(d). The values of α_{1n} , α_{2n} and ρ_n are chosen accordingly to stability condition of the transfer functions $H_{cl}(z)$ and $H_{cl}(s)$ shown in equations (6) and (9).

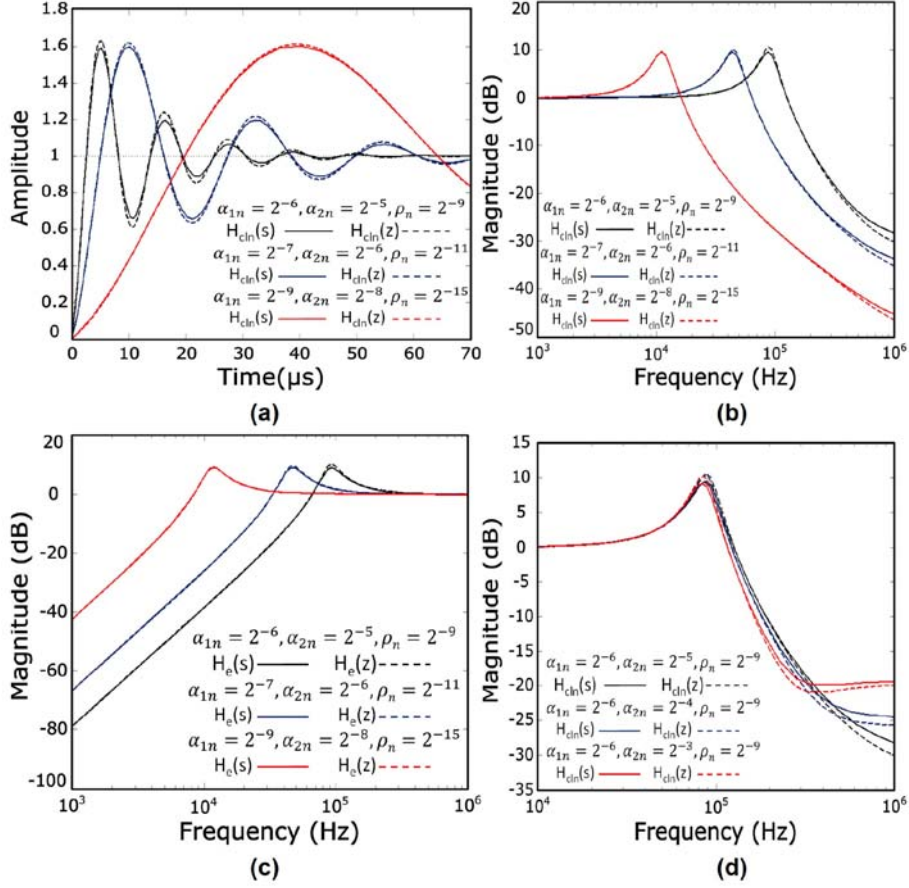


Figure 3. Comparison of: (a) step response, (b) magnitude responses of closed-loop transfer functions $H_{cln}(z) = H_{cl}(z)/N$ and $H_{cln}(s) = H_{cl}(s)/N$, (c) magnitude responses of error transfer functions $H_e(z) = 1 - H_{cl}(z)/N$ and $H_e(s) = 1 - H_{cl}(s)/N$ and (d) magnitude responses of $H_{cln}(z)$ and $H_{cln}(s)$ for different α_{2n} factors.

4. Behavior-level Simulation

In this work, we used Verilog and Verilog-A to model the ADPLL blocks in 130-nm CMOS technology and simulate using Cadence AMS simulator. For modeling, we have incorporated two-stage PPF for DCO

with tuning range of 378-419MHz. The DCO is controlled by 4-bit integer and 7-bit fractional codes ($B_{frac} = 7$). The DCO with fractional control code has a third-order feed-forward $\Delta\Sigma$ -modulator and a dynamic-element-matching processing unit [14]. The resistor and capacitor values of the PPF shown in Figure 1(b) are $R_{1p} = 100\Omega$, $R_{2p} = 82\Omega$ and $C_{1p} = C_{2p} = 4.42\text{pF}$. The 64-phase PI shown in Figure 1(c) is adopted for this work with each branch resistor values of $R_1 = 1.8\text{k}\Omega$, $R_2 = 1.53\text{k}\Omega$, $R_3 = 1.34\text{k}\Omega$, $R_4 = 1.2\text{k}\Omega$, $R_5 = 1.1\text{k}\Omega$, $R_6 = 1.04\text{k}\Omega$, $R_7 = 1\text{k}\Omega$, $R_8 = 985\Omega$.

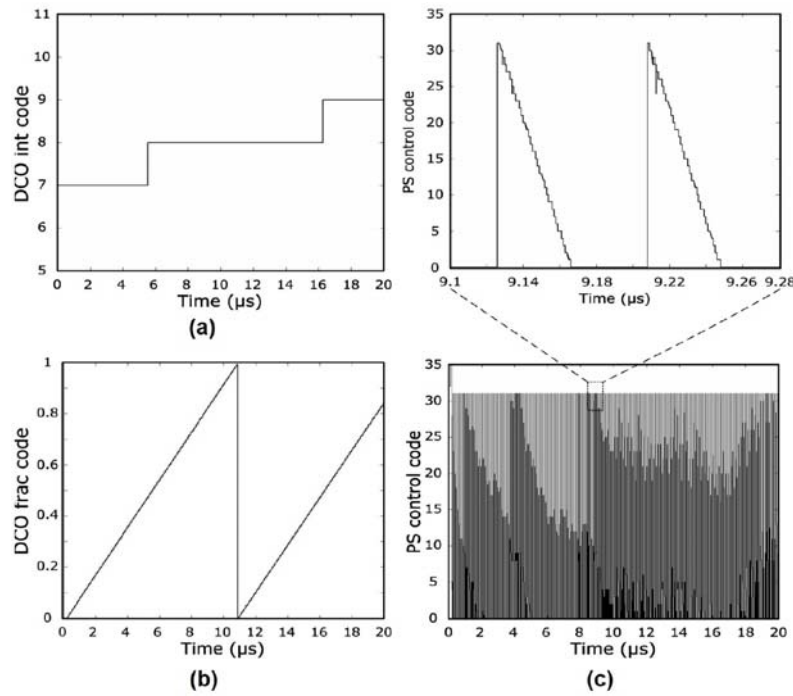


Figure 4. Control code variations with time: (a) DCO integer code decimal value, (b) DCO fractional code decimal value and (c) PS control code decimal value.

The DCO integer and fractional bit code changes for a step input are shown in Figures 4(a) and 4(b) as decimal value variations. The PS control

code with time to reduce the phase error is shown in Figure 4(c) as decimal variation. Figure 5(a) shows the time response of ADPLL output for the same step input, which shows the steady-state DCO frequency is about 393MHz. As shown in Figure 5(b), the output frequency settling to 393MHz is around 265nsec. Although this settling includes the initial start-up time of the DCO, it is comparable to the settling time estimated with the small-signal approximation model in Section 3, as described later.

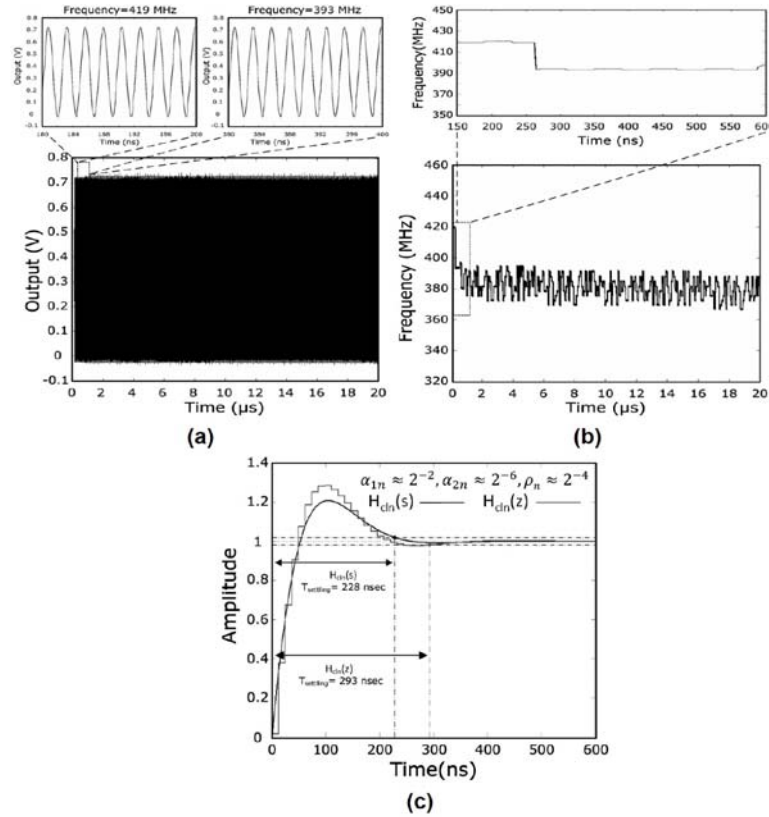


Figure 5. (a) ADPLL output waveform, (b) ADPLL output frequency versus time and (c) step responses of the $H_{cln}(z)$ and $H_{cln}(s)$ with extracted simulation parameters.

The value of K_{DCO} from simulations is about 3MHz/code change ($= 6\pi$ Mrps/code change), $K_{PPF+PI} = 2\pi/64$ is considered for the 64-phase

PI, and a divide-by-32 divider is used ($N = 32$) in the present design. The settling time of a second-order system is given by $T_{settling} = 4/\zeta\omega_n$, where damping factor $\zeta = 0.7$ is used as a good compromise between rise time and settling time with a single peak. Calculating ω_n from the above expression and substituting in equations (11) and (12), the loop filter parameters are calculated as $\alpha_1 = 2^{-18}$, $\alpha_2 = 5$, $\rho = 2^{-20}$ ($\alpha_{1n} \approx 2^{-2}$, $\alpha_{2n} \approx 2^{-6}$, $\rho_n \approx 2^{-4}$). These values correspond to a stable system from the conditions mentioned in Subsection 3.1. Figure 5(c) shows the step response of the closed-loop transfer functions $H_{cIn}(z)$ and $H_{cIn}(s)$ from the modeling with settling times of 228nsec and 293nsec which is close to the settling time simulated using the behavior-level simulation (about 265nsec). The z - and linearly approximated s -domain models have close agreement against the behavior-level simulation result.

As shown in Figure 5(b), there is steady-state frequency variation of the ADPLL output. This is attributed to the small frequency division ratio N for simulation time reduction in this study. By using a divider configuration with higher division ratios [22], the residual frequency variation of the ADPLL output can be reduced easily.

5. Conclusion

In this paper, comprehensive z -domain and its linearly approximated s -domain models of a controller-based ADPLL with phase selection mechanism are presented, and using the classical two-pole control system transfer function, the characteristics of the system are verified. The proposed ADPLL loop stability is independent of PVT, and the phase and frequency errors are eliminated by the closed-loop system for a phase and frequency step input. Inclusion of phase selection factor reduces the residual phase error of the system. The modeling has been validated against behavior-level simulation on 130-nm CMOS technology with a supply voltage of 0.7V using Cadence AMS simulator.

Acknowledgment

This study is supported by the VLSI Design and Education Center (VDEC), University of Tokyo in collaboration with Cadence Design Systems.

References

- [1] K. Muhammad, R. B. Staszewski and D. Leipold, Digital RF processing: toward low-cost reconfigurable radios, *IEEE Commun. Mag.* 43(8) (2005), 105-113.
- [2] L. Maurer, R. Stuhlberger, C. Wicpalek, G. Haberpeuntner and G. Hueber, Be flexible, *IEEE Microwave Magazine* 9(2) (2008), 83-95.
- [3] R. B. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J. L. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. E. Eliezer, E. de-Obaldia and P. T. Balsara, All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS, *IEEE J. Solid-State Circuits* 39(12) (2004), 2278-2291.
- [4] C. Wicpalek, T. Mayer, L. Maurer, U. Vollenbruch, Y. Liu and A. Springer, Analysis and measurement of spurious emission and phase noise performance of an RF all-digital phase locked loop using a frequency discriminator, *IEEE/MTT-S International Microwave Symposium*, Jun. 2007, pp. 2205-2208.
- [5] T.-Y. Hsu, B.-J. Shieh and C.-Y. L. Lee, An all-digital phase-locked loop (ADPLL)-based clock recovery circuit, *IEEE J. Solid-State Circuits* 34(8) (1999), 1063-1073.
- [6] C.-C. Chung and C.-Y. Lee, An all-digital phase-locked loop for high-speed clock generation, *IEEE J. Solid-State Circuits* 38(2) (2003), 347-351.
- [7] N. D. Dalt, A design-oriented study of the nonlinear dynamics of digital bang-bang PLLs, *IEEE Trans. Circuits Syst. I* 52(1) (2005), 21-31.
- [8] N. D. Dalt, E. Thaller, P. Gregorius and L. Gazsi, A compact triple-band low-jitter digital LC PLL with programmable coil in 130-nm CMOS, *IEEE J. Solid-State Circuits* 40(7) (2005), 1482-1490.
- [9] Y. Makihara, M. Ikebe and E. Sano, Evaluation of digitally controlled PLL by clocked-period comparison, *IEICE Trans. Electron.* E90-C(6) (2007), 1307-1310.

- [10] D. Miyashita, H. Kobayashi, J. Deguchi, S. Kousai, M. Hamada and R. Fujimoto, A -104dBc/Hz in-band phase noise 3GHz all digital PLL with phase interpolation based hierarchical time to digital converter, *IEICE Trans. Electron.* E95-C(6) (2012), 1008-1016.
- [11] F. M. Gardner, *Phase Lock Techniques*, 3rd. ed., John Wiley and Sons, 2008.
- [12] R. B. Staszewski and P. T. Balsara, Phase-domain all-digital phase-locked loop, *IEEE Trans. Circuits and Systems II* 52(3) (2005), 159-163.
- [13] J. G. Maneatis, Low-jitter process-independent DLL and PLL based on self-biased techniques, *IEEE J. Solid-State Circuits* 31(11) (1996), 1723-1732.
- [14] G. Tsuruyama, H. Ham, J. Wang, T. Matsuoka and K. Taniguchi, Analysis on influence of capacitor switching in digitally-controlled oscillator using behavior-level simulation, *IEICE Trans. Fundamentals* J94-A(2) (2011), 145-148 (in Japanese).
- [15] M. J. Gingell, Single sideband modulation using sequence asymmetric polyphase networks, *Electrical Communication* 48(1-2) (1973), 21-25.
- [16] F. Behbahani, Y. Kishigami, J. Leete and A. A. Abidi, CMOS mixers and polyphase filters for large image rejection, *IEEE J. Solid-State Circuits* 36(6) (2001), 873-887.
- [17] S. J. Fang, A. Bellaouar, S. T. Lee and D. J. Allstot, An image-rejection down-converter for low-IF receivers, *IEEE Trans. Microwave Theory and Tech.* 53(2) (2005), 478-487.
- [18] H. Chung, D.-K. Jeong and W. Kim, An 128-phase PLL using interpolation technique, *J. Semiconductor Technology and Science* 3(4) (2003), 181-187.
- [19] S. Hwang, J. Moon and M. Song, Design of a 1.8V 6-bit folding interpolation CMOS A/D converter with a $0.93[\text{pJ/convstep}]$ figure-of-merit, *IEICE Trans. Electron.* E91-C(2) (2008), 213-219.
- [20] W. Liu, W. Li, P. Ren, C. L. Lin, S. D. Zhang and Y. Y. Wang, A PVT tolerant 10 to 500MHz all-digital phase-locked loop with coupled TDC and DCO, *IEEE J. Solid-State Circuits* 45(2) (2010), 314-321.
- [21] E. I. Jury, A note on the modified stability table for linear discrete time systems, *IEEE Trans. Circuits and Systems* 38(2) (1991), 221-223.
- [22] R. Saichandrateja, J. Bae, I. Jo, T. Kihara and T. Matsuoka, A low-power CMOS programmable frequency divider with novel retiming scheme, *IEICE Electronics Express* 12(6) (2015), 20141233.